

***Remarks***

Reconsideration of this Application is respectfully requested.

Applicants respectfully thank the Examiner for extending the courtesy of a telephonic interview to Applicants' representatives on January 8, 2008. Applicants' representatives found the Examiner's comments to be very helpful and instructive.

Upon entry of the foregoing amendment, claims 1-20 are pending in the application, with claims 1, 12 and 17 being the independent claims. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

***Claim Objections***

The Examiner objected to claims 17-20 because of language informalities. Claim 17 has been amended per the Examiner's suggestions for the purposes of consistency. Therefore, Applicants respectfully request the objections to claims 17-20 be withdrawn.

***Rejections under 35 U.S.C. § 112***

The Examiner rejected claims 1-20 under 35 U.S.C. § 112 as failing to comply with the written description requirement. Claims 1 and 12 have been amended to include the language "wherein the first signal line and the second signal line are configured to communicate audio; wherein the audio is communicated devoid of a third signal line that carries data different from the audio information segments transmitted on the first signal line or different from the number of synchronization markers transmitted on the second

signal line." Likewise, claim 17 has been amended to include the language "wherein the two-line audio information segments are configured to transfer audio data; wherein the audio data is transferred devoid of a third signal line that carries data different from the audio information segments transmitted on the data line or different from the number of sync pulses transmitted on the synchronization line." The above recited features are discussed, for example, in Applicants' specification in paragraph 0026, where it is stated "the 2-line MAI bus of FIG. 2 can be used to transfer digitized data samples of any audio data rate, or a compressed audio bit stream of any rate," and "the number of data lines can be reduced from 3 to 2." These features are also illustrated in FIGs. 2-3.

With respect to FIG. 1, FIG. 1 is an example of conventional art. Note that when introducing FIG. 1 in paragraph [0021], FIG. 1 is not identified as an embodiment of the present invention. FIG. 1 is an example an I<sup>2</sup>S system, whereas "the present invention is directed to improved methods and systems" (see specification, paragraphs [0025]-[0026]). FIG. 1 has been amended to clarify this issue, as noted above.

With respect to FIG. 2, synchronization line 207 and data line 208 do not carry four different types of data on the signal lines. Even though both synchronization line 207 and data line 208 branch off to different receivers, the data carried on each branch for each respective line is the same. And as stated in the specification, "the system 200 also optionally includes additional destination devices such as an additional receiver 224" (see paragraph [0030]). Synchronization line 207 and data line 208 travel directly to receiver 204 if receiver 224 is not included, meaning synchronization line 207 and data line 208 are configured to communicate audio, wherein the audio is communicated devoid of a third signal line.

Therefore, amended claims 1, 12, and 17 comply with the written description requirement. Applicants respectfully request that the rejection of claims 1, 12, and 17 be withdrawn.

Claims 2-11 depend from claim 1, claims 13-16 depend from claim 12, and claims 18-20 depend from claim 17. Therefore, Applicants respectfully request that the rejection of claims 2-11, 13-16, and 18-20 be withdrawn.

***Rejections under 35 U.S.C. § 102***

The Examiner rejected claims 1-4, 6, 8-14, and 16-19 under 35 U.S.C. § 102(b) as being anticipated by CS4205 (CrystalClear Audio Codec '97 product information document, hereinafter "CrystalClear"). Applicants traverse the rejection of claims 1-4, 6, 8-14, and 16-19 because the cited reference fails to disclose, teach, or suggest all of the features of the claimed invention.

For example, the cited reference fails to disclose, teach, or suggest a method for communicating audio, "wherein the first signal line and the second signal line are configured to communicate audio; wherein the audio is communicated devoid of a third signal line that carries data different from the audio information segments transmitted on the first signal line or different from the number of synchronization markers transmitted on the second signal line," as recited in claim 1. Claims 12 and 17 recite similar features.

In CrystalClear, however, at least three wires carrying three different types of data are necessary for proper transmission. The CS4205 audio codec communicates with two main components: a DC '97 controller and stereo ADCs/DACs (see figure 16). As stated in CrystalClear, the DC '97 (also known as the Digital AC '97) controller "is

responsible for all communications between the CS4205 and the remainder of the system" (see section 2, page 13). And as stated in CrystalClear, "all communication with the CS4205 is established with a 5-wire digital interface to the controller called the AC-link" (see section 2.1, page 13). That is, in CrystalClear, five lines are present for communication. This is illustrated in figure 7. Also, "all clocking for the serial communication is synchronous to the BIT\_CLK," and the "BIT\_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs" (see section 2.1, page 13).

More specifically, CrystalClear teaches of a five line digital interface between the CS4205 and the DC '97 controller, and at least three of these wires carrying different data are necessary for proper transmission. The following three wires are necessary (see section 4, page 19, figure 14):

- (1)     **BIT\_CLK**: Because the CS4205 audio codec generates its own clock signal and all communication is synchronous with this clock signal, the CS4205 audio codec must transmit this clock signal, BIT\_CLK, to all relevant components.
- (2)     **SYNC**: The SYNC line is necessary to indicate the type of data being sent over SDATA\_OUT or SDATA\_IN.
- (3)     **SDATA OUT / SDATA IN**: Necessary to transmit the audio data.

Figure 14 illustrates the serial port timing during both serial data output and input frames as noted in the first paragraph of section 4.1 and the first paragraph of section 4.2. While one component, either the CS4205 or the DC '97 controller, may be transmitting a total of two data or timing signals at any given time, the two data or timing signals are not configured to communicate audio, where the audio is communicated devoid of a third

signal line that carries data different from the data carried on the two data or timing signal lines. For example, during SDATA\_OUT transmission, the DC '97 controller transmits the SYNC signal and the SDATA\_OUT signal to the CS4205, but receives the BIT\_CLK signal to ensure proper audio communication.

Now looking at the interface between the CS4205 and the stereo DAC, at least three signal lines are necessary for audio communication:

(1) **SCLK / MCLK**: One of SCLK or MCLK is necessary because both signals are a function of BIT\_CLK, as CrystalClear states " SCLK will be 64 Fs (BIT\_CLK/4)" and "the existing 256 Fs BIT\_CLK will be used as MCLK" (see section 6.1, page 54). As mentioned above, BIT\_CLK (or a signal derived from it), must be transmitted from the CS4205 to any relevant component to maintain synchronization. The Examiner noted that SCLK may be optional. In this case, "SCLK is internally derived from MCLK and LRCLK" (see section 6.1, page 54), meaning at least MCLK and LRCLK are necessary.

(2) **LRCLK**: LRCLK is necessary to indicate whether the data being communicated refers to a left or right channel.

(3) **SDOUT**: SDOUT is analogous to SDATA\_OUT or SDATA\_IN in that the line transmits data.

The interface between CS4205 and stereo ADC is similar to the interface with stereo DAC, except stereo ADC transmits data back to the audio codec via SDI1, SDI2, or SDI3 (see figure 16). Three lines again are still necessary:

(1) **SCLK / MCLK**

(2) **LRCLK**

(3) **SDI1 / SDI2 / SDI3**

Since the stereo ADC must be notified what channel data to send and for how long, LRCLK is needed, and since it must be synchronized with the CS4205, at least SCLK or MCLK is needed. Again, the CS4205 transmits SCLK/MCLK and LRCLK, however the signal lines are not configured to communicate audio, where the audio is communicated devoid of a third signal line that carries different data. In this case SDI1/SDI2/SDI3 is the third signal line.

For at least these reasons, Applicants respectfully submit that claim 1 is not anticipated by CrystalClear since claim 1 recites that "the first signal line and the second signal line are configured to communicate audio; wherein the audio is communicated devoid of a third signal line that carries data different from the audio information segments transmitted on the first signal line or different from the number of synchronization markers transmitted on the second signal line," whereas CrystalClear requires a minimum of three lines carrying three different types of data. Applicants therefore respectfully request that the rejection of claim 1 be withdrawn.

Claims 2-4, 6, and 8-11 depend from claim 1, and are patentable for at least the same reasons as discussed with claim 1, and further in view of their own respective features.

As noted above, claims 12 and 17 contain similar language as claim 1 and are therefore allowable for at least the same reasons as discussed with claim 1. Applicants, therefore, respectfully request that the rejection of claims 12 and 17 be withdrawn.

Claims 13-14, 16, and 18-19 respectively depend from claims 12 and 17, and therefore also allowable at least the reasons claims 12 and 17 are allowable, and further in view of their own respective features.

***Rejections under 35 U.S.C. § 103***

Claims 5, 15, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over CrystalClear in view of U.S. Patent No. 7,088,398 to Wolf et al. (hereinafter "Wolf"). Claim 5 depends ultimately from claim 1, claim 15 depends ultimately from claim 12, and claim 20 depends ultimately from claim 17. Wolf does not overcome all of the deficiencies of CrystalClear relative to claims 1, 12, and 17, described above. For at least these reasons and further in view of their own features, claims 5, 15, and 20 are patentable over the combination of CrystalClear and Wolf. Reconsideration and withdrawal of the ground of rejection is therefore respectfully requested.

Claim 7 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over CrystalClear in view of U.S. Patent No. 6,006,287 to Wakazu (hereinafter "Wakazu"). Claim 7 depends ultimately from claim 1. Wakazu does not overcome all of the deficiencies of CrystalClear relative to claim 1, described above. For at least these reasons and further in view of their own features, claim 7 is patentable over the combination of CrystalClear and Wakazu. Reconsideration and withdrawal of the ground of rejection is therefore respectfully requested.

***Conclusion***

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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